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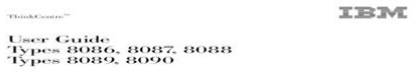

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When the queue is empty, instructions take as long to complete as they take to fetch. Both the 8086 and 8088 take four clock cycles to complete a bus cycle; whereas for the 8086 this means four clocks to transfer two bytes, on the 8088 it is four clocks per byte. Therefore, for example, a twobyte shift or rotate instruction, which takes the EU only two clock cycles to execute, actually takes eight clock cycles to complete if it is not in the prefetch queue. A sequence of such fast instructions prevents the queue from being filled as fast as it is drained, and In short, an 8088 typically runs about half as fast as 8086 clocked at the same rate, because of the bus bottleneck the only major difference.When programming the 8088, for CPU efficiency, it is vital to interleave longrunning instructions with short ones whenever possible. For example, a repeated string operation or a shift by three or more will take long enough to allow time for the 4byte prefetch queue to completely fill. If short instructions i.e. ones totaling few bytes are placed between slower instructions like these, the short ones can execute at full speed out of the queue. If, on the other hand, the slow instructions are executed sequentially, back to back, then after the first of them the bus unit will be forced to idle because the queue will already be full, with the consequence that later more of the faster instructions will suffer fetch delays that might have been avoidable. If those code segments are the bodies of loops, the difference in execution time may be very noticeable on the human timescale.The same ALU that is used to execute arithmetic and logic instructions is also used to calculate effective addresses. There is a separate adder for adding a shifted segment register to the offset address, but the offset EA itself is always calculated entirely in the main ALU.

Furthermore, the loose coupling of the EU and BIU bus unit inserts communication overhead between the units, and the fourclock period bus transfer cycle is not particularly streamlined. Contrast this with the twoclock period bus cycle of the 6502 CPU and the 80286s threeclock period bus cycle with pipelining down to two cycles for most transfers. Most 8088 instructions that can operate on either registers or memory, including common ALU and datamovement operations, are at least four times slower for memory operands than for only register operands. Therefore, efficient 8088 and 8086 programs avoid repeated access of memory operands when possible, loading operands from memory into registers to work with them there and storing back only the finished results. The relatively large general register set of the 8088 compared to its contemporaries assists this strategy. When there are not enough registers for all variables that are needed at once, saving registers by pushing them onto the stack and popping them back to restore them is the fastest way to use memory to augment the registers, as the stack PUSH and POP instructions are the fastest memory operations. The same is probably not true on the 80286 and later; they have dedicated address ALUs and perform memory accesses much faster than the 8088 and 8086.All jumps and calls take at least 15 clock cycles. Any conditional jump requires four clock cycles if not taken, but if taken, it requires 16 cycles in addition to resetting the prefetch queue; therefore, conditional jumps should be arranged to be not taken most of the time, especially inside loops. In some cases, a sequence of logic and movement operations is faster than a conditional jump that skips over one or two instructions to achieve the same result. Many simple multiplications by small constants besides powers of 2, for which shifts can be used can be done much faster using dedicated short subroutines.Retrieved 1 June 2019.

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Speeds in Mobile Computing Applications Intel AR717 The Many Facets of Flash Memory Intel AR718 Standardizing on a Flash File System Intel AR723 Interfacing BootBlock Flash Memories to the MCSr 96 Family. The algorithms are based on the knowledge of some timing and control information available to users through microprocessor manuals and data sheets. The tests are functional in nature. We also establish the order of complexity of the algorithms presented in this paper. As an example, the test complexity for a microprocessor is computed and the results are compared with a known algorithm. Previous article in issue Next article in issue Download full text in PDF Recommended articles Citing articles 0. This work is in part supported by the U.S. Army Communication Electronics Command under Research Contract No. Recommended articles No articles found. Citing articles Article Metrics View article metrics About ScienceDirect Remote access Shopping cart Advertise Contact and support Terms and conditions Privacy policy We use cookies to help provide and enhance our service and tailor content and ads. By continuing you agree to the use of cookies. USER SYSTEM PACKAGE Data Sheet Tracks 176 report themselves as 075 SD Manual Text Only Fact Sheet Magnetic ISSCC Panel Discussion With Complete Training and Support Systems System 2nd edition by Rebecca Thomas, Ph.D. and Jean Yates, March 1971 SX CPU PC Designs Using FlashFile.

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Intelevision. Intellec Library Manager Micromap. Multibus. Multimodule Table of Contents Functional Distribution 11. Microprocessors 12. Interrupt Controller 13. Bus Interface Components 13. Multiprocessing 13. Bus Organization 14. Local Bus 14. System Bus 15. Processing Modules 16. Bus Implementation Examples 16. Development Aids 112 Processor Architecture 23. Execution Unit 25. Bus Interface Unit 25. General Registers 26. Segment Registers 27. Instruction Pointer 27. Flags 27. Mode Selection 28. Memory 28. Storage Organization 28. Segmentation 210. Physical Address Generation 211. Dynamically Relocatable Code 213. Stack Implementation 214. Dedicated and Reserved Memory Locations.... 214. Direct Memory Access 217. Multiprocessing Features 217. Bus Lock 217. WAIT and TEST 218. Escape 219 Processor Control and Monitoring 222. Interrupts 222.

External Interrupts 222. Internal Interrupts 224. Interrupt Pointer Table 225. Interrupt Procedures 226. SingleStep Trap Interrupt 228. Breakpoint Interrupt 228. System Reset 229. Instruction Queue Status 229. Processor Halt 229. Status Lines 230. Instruction Set 230. Data Transfer Instructions 231. General Purpose Data Transfers 231. Address Object Transfers 232. Flag Transfers 232. Arithmetic Instructions 233. Arithmetic Data Formats 233. Arithmetic Instructions and Flags 234. Addition 235. Subtraction 236. Multiplication 236. Division 237. Bit Manipulation Instructions 238. Logical 238. Shifts 239. Rotates 239. String Instructions 240. Program Transfer Instructions 243. Unconditional Transfers 243. Conditional Transfers 245. Iteration Control 245. Interrupt Instructions 246. Processor Control Instructions 247. Flag Operations 247. External Synchronization 248. No Operation 248. Instruction Set Reference Information 248. Addressing Modes 268. Register and Immediate Operands 268. Memory Addressing Modes 268. The Effective Address 268. Direct Addressing 269. Register Indirect Addressing 269. Based Addressing 270.

Indexed Addressing 270 String Addressing 272. Programming Facilities.. 272. Software Development Overview 273. Statements and Comments 275. Data Definition 275. Assignment Statement 277. Program Flow Statements 279. Procedures 281 Constants 284. Defining Data 285. Records 285. Structures 287. Addressing Modes 287. Segment Control. 288. Procedures 290 Programming Guidelines and Examples 296. Programming Guidelines 296. Segments and Segment Registers. 296. SelfModifying Code 296. Operating Systems. 297. Interrupt Service Procedures 299. StackBased Parameters 2100. Flag Images 2100. Programming Examples 2100. Procedures. 2100. Jumps and Calls 2105. Records 2110. Dynamic Code Relocation 2113. Breakpoints 2117. Interrupt Procedures.. 2119. String Operations 2125 Evolution 31. Principles of Operation 32. Channels 34. Channel Programs Task Blocks 34 Bus Configurations 35. A Sample Transaction 310. Applications 312. Processor Architecture 313. Common Control Unit CCU 313. Instruction Fetch Unit 314. Bus Interface Unit BIU 316. Channels 316. Registers 317. Program Status Word 318. Tag Bits 319. Concurrent Channel Operation 320. Memory 321. Storage Organization 322. Dedicated and Reserved Memory Locations 323. Dynamic Relocation 323. Memory Access 324. Device Addressing 326. DMA Transfers. 327. Preparing the Device Controller. 327. Preparing the Channel 327. Beginning the Transfer 331. DMA Transfer Cycle.. 332. Following the Transfer 333. Multiprocessing Features 334. Bus Arbitration 334 Bus Arbitration for IOP Configurations 336. Bus Load Limit 336. Bus Lock 337. Processor Control and Monitoring 337. Initialization 337. Channel Commands 340. DRQ DMA Request 343. EXT External Terminate 343. Interrupts 343. Status Lines 343. Instruction Set 344. Data Transfer Instructions, 344. Arithmetic Instructions 345. Logical and Bit Manipulation Instructions 346. Program Transfer Instructions 348. Processor Control Instructions 349.

Instruction Set Reference Information 351 Register and Immediate Operands 359. Memory Addressing Modes 359. The Effective Address 360. Based Addressing 360. Offset Addressing 360. Indexed Addressing 360. Indexed AutoIncrement Addressing 361. Programming Facilities 363 Constants 366. Defining Data 366. Structures 367. Addressing Modes 368. Program Transfer Targets 368. Procedures 369. Segment Control 369. Intermodule Communication 370. Sample Program 373. Linking and Locating ASM89 Modules 376. Programming Guidelines and Examples 379. Programming Guidelines 379. Segments 379. SelfModifying Code 379. Programming Examples 381. Initialization and Dispatch 381. MemorytoMemory Transfer 385. Saving and Restoring Registers 385 CPU Architecture 41. Bus Operation 45. Clock Circuit 410. Minimum Mode 411. Maximum Mode 411. External Memory Addressing 414. Interrupts 416. Machine Instruction Encoding and Decoding.. 418 System Configuration 439. Local Mode 439. Remote Mode 440. Bus Operation. 441. Initialization 444 DM A Termination 450. Peripheral Interfacing 450. Instruction Encoding 452 AP61 Multitasking for the 8086 A67. AP50 Debugging Strategies and. Considerations for 8089 Systems A85. AP5 1 Designing 8086, 8088, 8089. Multiprocessing Systems with the 8289. Bus Arbiter Alll. AP59 Using the 8259A Programmable. Interrupt Controller A 1 3 5. Vehicle for Executing 8086. Program Code A209 Microprocessor Bl. M8086 16Bit HMOS Microprocessor B22

M8284 Clock Generator and Driver for DMA Controller B92. Interrupt Controller Bl 06 Interface.... B131. Interface B133. Disk Controller B 1 34. Controller. B135 Interface B137 RAM Memories EPROM Memories Power PROM B148. Development Tools. Microcomputer Development System B149. Development Package B153 Chapter 1. Introduction The manual is intended to Recognizing that successful microcomputerbased Additional references, available from Intels.

Literature Department, are cited in the program The manual contains four chapters and three Chapter 2 describes the 8086 and 8088 Central. Processing Units, and Chapter 3 covers the 8089. These two chapters are Appendix A is a collection of 8086 family applica Considered individually, the 8086, 8088 and 8089 Moreover, these processors are elements of a The components in the 8086 family have been In this way a single Finally, the modular structure of the family The 8086 family architecture is characterized by Functional Distribution. Table 11 lists the components that constitute the All components are Microprocessor. Technology Pins. Description Support Component. Technology. Pins. Function Octal Latch Inverting. Bipolar Bipolar Octal Bus Transceiver Inverting. Bipolar Bipolar Bipolar Microprocessors. At the core of the product line are three The 8086 and 8088 are thirdgeneration central The 8088 transfers data Controller assumes responsibility for controlling CPU pins no CPUs. They may also transfer data by DMA, at Interrupt Controller. The 8259A Programmable Interrupt Controller The 8259 A accepts Each interrupt Bus Interface Components. Components may be selected from this modular All of the bus The 8284 Clock Generator and Driver provides Two latches The 8288 Bus Controller decodes status signals The 8289 Bus Arbiter controls the access of a pro Arbiters for each Multiprocessing. Employing multiple processors in medium to The 8086 family architecture is explicitly designed The architecture supports two types of pro The 8086 architecture also supports a second type Coprocessor A coprocessor dif The 8086 family architecture provides builtin In all cases, the arbitra For mutual exclusion, each processor has a. LOCK bus lock signal which a program may The 8089 may lock the This instruction can be Bus Organization. Figure 11 summarizes the 8086 family bus struc The 8086 family Local Bus.

The local bus is optimized for use by the 8086 Since standard memory This allows Both independent processors and coprocessors Because the processors on the local bus share the JprocessorJ J PROCESSOR j System Bus. A full implementation of an 8086 system bus con These signals are designed to meet the needs of The system bus design is modular and subsets A group of bus interface components transforms Processing Modules. The processors and bus interface groups that Arbiters in each processing module control the A second bus interface group may be connected If processor programs Bus Implementation Examples. This section summarizes the 8086 family bus Note that these In its minimum mode configuration, the 8088 These peripherals contain Two latches provide an This demulti CPU. Eightbit peripherals may be connected to Including an 8259 A gives The minimum mode The processors all share Arbitration logic built The 8289 enables highperformance systems to be Several different combinations of processors may All of the processors on the local bus obtain One or two 8089s in a multimaster processing Memory, contain The IF statement figure 250 selects one or the IF relationalexpression. THEN statement!; If the rela Therefore, GOTO target; The statement A CALL statement written in the form. CALL procname parmlist; Thus, unlike a GOTO, Procedures Social Security and net pay. The organization of Procedures, then, provide A procedure usually is defined early in a program, A procedure Untyped pro CALL statements. Figure 255 shows how simple The statements forming the body of a procedure REENTRANT, making them concurrently usable Since the execution Examples of processor features not accessible An ASM86 program often can be written to For example, assume that the It is easier to write assembly language programs in. ASM86 than it is in many assembly languages. ASM86 contains powerful data structuring MOV destinationoperand, sourceoperand.

The assembler generates the correct machine Finally, the ASM86 Statements. Compared to many

assemblers, ASM86 accepts a In particular, Blanks may be inserted All ASM86 statements are classified as instruc ASM86 instruction produces one machine ASM86 instructions are written in the form Zero, one or two operands Finally, writing a semicolon signifies that what Comments do not affect Writing a directive gives ASM86 information to About 20 dif Some directives require a name to be present, ASM86 recognizes A comment may be written as the last field of a Some of the more commonly used directives Constants. Binary, decimal, octal and hexadecimal numeric ASM86 statements; the assembler can perform Negative numbers are assembled in standard Character constants are enclosed in single quotes When used as immediate Defining Data.